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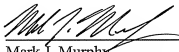
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in the following listed application(s) or patent(s) for which the issue fee has been paid.

<u>Patent No.</u>	<u>Serial No.</u>	<u>Patent Date</u>	<u>US Filing Date</u>	<u>Confirmation No.</u>	<u>Attorney Docket No.</u>
7,245,018 B1	09/598,736	07/17/2007	06/21/2000	5820	0553-0189

Respectfully Submitted,



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(12) **United States Patent**
Takayama et al.(10) **Patent No. US 7,245,018 B1**
(45) **Date of Patent: Jul. 17, 2007**(54) **WIRING MATERIAL, SEMICONDUCTOR
DEVICE PROVIDED WITH A WIRING
USING THE WIRING MATERIAL AND
METHOD OF MANUFACTURING THEREOF**5,594,569 A 1/1997 Konuma et al. 349/122
5,643,826 A 7/1997 Ohtani et al. 437/88
5,667,665 A 9/1997 Shindo et al. 205/589
5,738,948 A 4/1998 Ikeda et al. 428/663

(Continued)

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Sato, Kanagawa (JP); Shunpei
Yamazaki, Tokyo (JP)****FOREIGN PATENT DOCUMENTS**

JP 5-263226 10/1993

(Continued)

(73) Assignee: **Semiconductor Energy Laboratory
Co., Ltd. (JP)****OTHER PUBLICATIONS**(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.Yoshida, T. et al, "A Full Color Thresholdless Antiferroelectric LCD
Exhibiting Wide Viewing Angle with Fast Response Time," *SID 97
Digest*, pp. 841-844, 1997.

(Continued)

(21) Appl. No.: **09/598,736***Primary Examiner*—Hung Vu(22) Filed: **Jun. 21, 2000**(74) *Attorney, Agent, or Firm*—Cook, Alex, McFarron,
Manzo, Cummings & Mehler, Ltd.(30) **Foreign Application Priority Data**Jun. 22, 1999 (JP) 11-175937
Jun. 29, 1999 (JP) 11-183258(57) **ABSTRACT**(51) **Int. CL**
H01L 23/48 (2006.01)
H01L 23/52 (2006.01)
(52) **U.S. CL** 257/763; 257/764; 257/770
(58) **Field of Classification Search** 257/763,
257/764, 770; 438/648, 649, 656, 683, 685
See application file for complete search history.A semiconductor device having good TFT characteristics is realized. By using a high purity target as a target, using a single gas, argon (Ar), as a sputtering gas, setting the substrate temperature equal to or less than 300° C., and setting the sputtering gas pressure from 1.0 Pa to 3.0 Pa, the film stress of a film is made from -1×10^{10} dyn/cm² to 1×10^{10} dyn/cm². By thus using a conducting film in which the amount of sodium contained within the film is equal to or less than 0.3 ppm, preferably equal to or less than 0.1 ppm, and having a low electrical resistivity (equal to or less than 40 $\mu\Omega\cdot\text{cm}$), as a gate wiring material and a material for other wirings of a TFT, the operating performance and the reliability of a semiconductor device provided with the TFT can be increased.(56) **References Cited****U.S. PATENT DOCUMENTS**4,619,695 A 10/1986 Oikawa et al. 75/65
4,770,948 A * 9/1988 Oikawa et al. 428/664
5,208,170 A 5/1993 Kobeda et al. 437/34
5,341,016 A * 8/1994 Prall et al. 257/412
5,477,359 A * 12/1995 Okazaki 349/130**46 Claims, 26 Drawing Sheets**